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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,312	05/17/2006	Yasuhiko Kasama	80751037	4635
466 YOUNG & TH	7590 06/12/2007 HOMPSON		EXAMINER	
745 SOUTH 23RD STREET			HO, ANTHONY	
2ND FLOOR ARLINGTON, VA 22202			ART UNIT	PAPER NUMBER
			2815	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
	10/568,312	KASAMA ET AL.				
Office Action Summary	Examiner	Art Unit				
	Anthony Ho	2815				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	correspondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DATE - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  If NO period for reply is specified above, the maximum statutory period was reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tir will apply and will expire SIX (6) MONTHS from a cause the application to become AB ANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 22 M	<u>ay 2007</u> .					
·—	,—					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 49	53 O.G. 213.				
Disposition of Claims						
4)⊠ Claim(s) <u>1-17</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6) Claim(s) <u>1-17</u> is/are rejected.						
7) Claim(s) is/are objected to.	u alastian vanuiramant					
8) Claim(s) are subject to restriction and/or	r election requirement.	•				
Application Papers						
9)☐ The specification is objected to by the Examine	r.					
10)⊠ The drawing(s) filed on <u>22 May 2007</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the	drawing(s) be held in abeyance. Se	e 37 CFR 1.85(a).				
Replacement drawing sheet(s) including the correct						
11)☐ The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12) ☐ Acknowledgment is made of a claim for foreign a) ☐ All b) ☐ Some * c) ☐ None of:	priority under 35 U.S.C. § 119(a	)-(d) or (f).				
<ol> <li>Certified copies of the priority documents</li> </ol>	s have been received.					
2. Certified copies of the priority documents	• •					
3. Copies of the certified copies of the prior	•	ed in this National Stage				
application from the International Bureau		ad.				
* See the attached detailed Office action for a list	or the certified copies not receive	eu.				
	`					
Attachment(s)	<del>-</del>	(DTO 440)				
Notice of References Cited (PTO-892)     Notice of Draftsperson's Patent Drawing Review (PTO-948)	4)					
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Informal F 6) Other:	Patent Application				

#### **DETAILED ACTION**

This is in response to amendment to application no. 10/568,312 filed on May 22, 2007. Claims 1-17 are presented for examination.

### Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The disclosure does not mention how one of ordinary skill in the art would be able to form the source and drain regions in the claimed linear device according to the drawings provided by the applicant.

These threaded devices with polymer organic semiconductors and isolation regions, etc. are theoretical. The complicated winding structures involving these materials for a working device have not been shown to work by experimental evidence. Applicant must submit experimental evidence showing a working device.

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Applicants argue that paragraph 0038 – paragraph 0040 enables the claimed invention, but applicants have not shown by experimental data that obtaining the claimed device is possible. There are no scientific literature that discusses such a device can be obtained. Therefore, the claimed invention is not enabled to one of ordinary skill in the art absent convincing evidence.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, as best understood, are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Solomon et al (US Patent 6,437,422).

In re claim 1, Solomon et al discloses a linear device including a gate electrode, a gate insulating region, a source region, a drain region, and a semiconductor region, characterized in that said semiconductor region is arranged between said source region comprising one or a plurality of source region(s) and said drain region comprising one or

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a plurality of drain region(s), in a radial direction within a cross section of a device region, so that a part of said gate insulating region is contacted with said semiconductor region (Figure 2). It would have been obvious from Solomon et al that a semiconductor region made of a semiconductor material would have a different conductivity type than those of the source and drain regions (column 8) since all conventional devices have source and drain regions of different conductivity type from the semiconductor region.

In re claim 2, Solomon et al discloses gate electrode and gate-insulating region are arranged inside or outside source region(s) and drain region(s) (Figure 2).

In re claims 3 and 6, Solomon et al discloses linear device comprises, at a center, one of: a hollow region; an electric conductor region; gate electrode; source region; drain region; another insulating region different from said gate insulating region; and another semiconductor region different from said semiconductor region (Figure 2).

In re claims 4 and 7-8, Solomon et al discloses linear device comprises a plurality of device regions through separation regions there between, respectively, in a longitudinal direction of a linear body constituting said linear device (Figure 2).

In re claims 5 and 9-11, Solomon et al discloses gate electrode, gate insulating region, source region(s), drain region(s), and/or semiconductor region constituting said linear

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device are formed of an organic semiconductor or electroconductive polymer (column 3 - column 4).

### Claim Rejections - 35 USC § 103

Claims 1-17, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon et al (US Patent 6,437,422) in view of Yamamoto (JP 2002-258775).

In re claim 1, Solomon et al discloses a linear device including a gate electrode, a gate insulating region, a source region, a drain region, and a semiconductor region, characterized in that said semiconductor region is arranged between said source region comprising one or a plurality of source region(s) and said drain region comprising one or a plurality of drain region(s), in a radial direction within a cross section of a device region, so that a part of said gate insulating region is contacted with said semiconductor region (Figure 2).

Yamamoto discloses the semiconductor region is made of a semiconductor material having a different conductivity type than those of the source and drain regions (Drawing 7; Drawing 9, Drawing 11; paragraph 0030 – paragraph 0083).

The advantage is to obtain a device with higher quality (paragraph 0008 – paragraph 0015).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the linear device as taught by Solomon et al with the semiconductor region is made of a semiconductor material having a different

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conductivity type than those of the source and drain regions as taught by Yamamoto in order to obtain a device with higher quality.

In re claim 2, Solomon et al discloses gate electrode and gate-insulating region are arranged inside or outside source region(s) and drain region(s) (Figure 2).

In re claims 3 and 6, Solomon et al discloses linear device comprises, at a center, one of: a hollow region; an electric conductor region; gate electrode; source region; drain region; another insulating region different from said gate insulating region; and another semiconductor region different from said semiconductor region (Figure 2).

In re claims 4 and 7-8, Solomon et al discloses linear device comprises a plurality of device regions through separation regions there between, respectively, in a longitudinal direction of a linear body constituting said linear device (Figure 2).

In re claims 5 and 9-11, Solomon et al discloses gate electrode, gate insulating region, source region(s), drain region(s), and/or semiconductor region constituting said linear device are formed of an organic semiconductor or electroconductive polymer (column 3 – column 4).

In re claims 12-14, Solomon et al discloses a linear device comprising; a longitudinally extended gate electrode surrounded by an annular gate insulator; a longitudinally

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extended annular semiconductor region surrounding said gate insulator; and an annular protection region surrounding the above regions (Figure 2).

Yamamoto discloses plural longitudinally extended first conductive regions; and a longitudinally extended second conductive region around said semiconductor region and separated from said plural first conductive regions by said semiconductor region (Drawing 7; Drawing 9, Drawing 11; paragraph 0030 – paragraph 0083).

The advantage is to obtain a device with higher quality (paragraph 0008 – paragraph 0015).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the linear device as taught by Solomon et al with plural longitudinally extended first conductive regions; and a longitudinally extended second conductive region around said semiconductor region and separated from said plural first conductive regions by said semiconductor region as taught by Yamamoto in order to obtain a device with higher quality.

In re claims 15-17, Solomon et al discloses a longitudinally extended first conductive region surrounded by an annular semiconductor region; and an annular protection region surrounding the above regions (Figure 2).

Yamamoto discloses a longitudinally extended annular gate insulator surrounding said semiconductor region; plural longitudinally extended second conductive regions, said plural second conductive regions being separated from each other so that a portion of said semiconductor region directly contacts said gate insulator between adjacent ones

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of said second conductive regions; and a longitudinally extended gate electrode surrounding said gate insulator (Drawing 7; Drawing 9, Drawing 11; paragraph 0030 paragraph 0083).

The advantage is to obtain a device with higher quality (paragraph 0008 – paragraph 0015).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the linear device as taught by Solomon et al with a longitudinally extended annular gate insulator surrounding said semiconductor region; plural longitudinally extended second conductive regions, said plural second conductive regions being separated from each other so that a portion of said semiconductor region directly contacts said gate insulator between adjacent ones of said second conductive regions; and a longitudinally extended gate electrode surrounding said gate insulator as taught by Yamamoto order to obtain a device with higher quality.

## Response to Arguments

Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

#### Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamagata et al (US Patent 4,983,539).

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Ho whose telephone number is 571-270-1432. The examiner can normally be reached on M-Th: 8:30AM-7:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH June 7, 2007

> JEROME JACKSON PRIMARY EXAMINER